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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,151	09/15/2003	Peter Poechmueller	INTECH 3.0-096 03 P 50757	2158

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EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,151	POECHMUELLER, PETER	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This office action is in response to Amendment filed on 05/24/2006. Claims 1-21 are pending in the application. All rejections and objections not explicitly repeated below are withdrawn.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4,6,8-15,17 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurjanowicz et al. US 6,894,941 B2, in view of Feurle et al., US 2003/0043674 A1.

Regarding claims 1 and 12, Kurjanowicz teaches that a method of reducing a rate for refreshing a portion of a dynamic random access memory (DRAM), comprising:

Providing a first portion of said DRAM comprising a plurality of volatile memory cells (it is taught as proving data in both memory banks 102 and 108 when DRAM operates in the long page access mode, col.7, lines 26-38 and col.8, lines 33-36) permitting refresh at a first rate (it is taught as refreshing at a first refresh rate in the single cell per bit mode; col.15, lines 37-39) and a second portion of said DRAM comprising a plurality of volatile memory cells (it is taught as proving data from upper memory bank 102 when DRAM operates in the short page access mode, col.7, lines 26-45 and col.8, lines 33-36) permitting refresh at a second rate (it is taught as refreshing at a second refresh rate in the two cells pre bit mode lower than said first rate; col.15, lines 40-43);

determining the first and second refresh rates that are permitted for the first and second portions (it is taught as determining the signal DIFF_MODE is at the low logic level or high logic level, if it is at low logic level, DRAM operates in the single cell access mode which the DRAM cells such as the cells in banks 102 and 108 are refreshed at a first refresh rate, if it is at high logic level, DRAM operates in the dual cell per bit access mode which the DRAM cells such as the cells in banks 102 are refreshed at a second refresh rate, col.7, lines 26-45, col.8, lines 13-17 and col.15, lines 36-42);

storing information (it is taught as DIFF_MODE signal and SHORT_PG SIGNAL, col.7, lines 26-45 and col.8, lines 13-36) for distinguishing between said first portion (it is taught as proving data in both memory banks 102 and 108 when DRAM operates in the long page access mode, col.7, lines 26-38 and col.8, lines 33-36) and said second portion of said DRAM (it is taught as proving data from upper memory bank 102 when

DRAM operates in the short page access mode, col.7, lines 26-45 and col.8, lines 33-36); and

accessing said stored information to determine when and to refresh said first portion at said first rate (it is taught as cases 1 and 2 as shown in table 1; see col.9, lines 39-55; Kurjanowicz clearly teaches when to refresh the first portion at said first rate, for example, when SHORT-PG and DIFF_MODE are at the low logic level) and to determine when and to refresh said second portion at said second rate (it is taught as cases 8 and 9 as shown table 1, see col.10, lines 20-45; Kurjanowicz clearly teaches when to refresh the second portion at said second rate, for example, when SHORT-PG and DIFF_MODE are at the high logic level).

Kurjanowicz does not clearly and specifically teach that a DRAM includes a first portion and a second portion which having **different plurality of memory cells** for different refresh rates. Kurjanowicz teaches that the first portion of DRAM can be considered as the memory cells of the upper memory bank 102 and the lower memory bank 108, and the second portion of DRAM can be considered as the memory cells of either the upper memory bank 102 and the lower memory bank 108 (see rejection of above).

However, Feurle teaches that a DRAM includes a first portion (Fig.1, one of four memory segments) and a second portion (Fig.1, one of four segments other than the first portion) which having different plurality of memory cells (see claim 1, each of word line and each bit line being respectively connected to memory cells of a single memory

segment) for different refresh rates (section 0046, memory segments 6b and 6d are be subjected to a refresh less frequently than the other memory segments 6a and 6c).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Feurle into Kurjanowicz's memory system such as a DRAM includes a first portion and a second portion which having different plurality of memory cells for different refresh rates because refresh times which vary on a segment-specific basis can be implemented in a way which is very easy and space-saving, and therefore cost-effective in terms of circuitry by cyclically addressing the memory segments and by the interruption, performed where necessary, of the passing on of the cyclically generated refresh instructions (section 0025, last seven lines).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claims 2 and 13, Kurjanowicz teaches said first portion and said second portion of said DRAM (Fig.3), and said information allows said first portion and said second portion to be distinguished (col.7, lines 26-45 and col.8, lines 33-36), Feurle further teaches said first portion and said second portion of said DRAM include one or more segments of said DRAM (Fig.1) and said first portion and said second portion are to be distinguished on the basis of said segments (it is taught as the time periods

between successive refreshed vary on a segment-specific basis, section 0025, first two lines).

Regarding claims 3 and 14, Kurjanowicz teaches that said first portion includes subportions (it is taught as logical sub-blocks, col.11, lines 47-48), at least some of said subportions being physically discontiguous (see Fig.6, it is taught as interleaved wordline architecture).

Regarding claims 4 and 15, Kurjanowicz teaches that said subportions are wordline spaces of said DRAM and said information allows said first portion and said second portion to be distinguished on the basis of said wordline spaces (Fig.6, col.11, lines 47-51).

Regarding claims 6 and 17, Kurjanowicz teaches the information is stored in said DRAM (Fig.3 and 4, According to the applicant's specification, the information is stored in the refresh map which connected to the segments, and Kurjanowicz also provide the DIFF_MODE signal and SHOR-PG having different access mode signals connected to the different banks).

Regarding claim 8, Kurjanowicz teaches that said information is stored on one or more fuses on an integrated circuit including said DRAM (col.3, lines 34-36).

Regarding claims 9 and 20, Kurjanowicz and Feurle teach that said information further allows a plurality of portions numbering one to n of said DRAM including said first portion and said second portion to be distinguished for refreshing said plurality of portions of said DRAM at a plurality of respective rates numbering one to n, and said stored information is accessed to refresh said plurality of portions at said respective rates including to refresh said first portion at said first rate, to refresh said second portion at said second rate, and to refresh said nth portion at said nth rate (it is taught as each segments is refreshed at a different rate, in this case, segments can be numbered from one to N, not only segments 6a to 6d; section 0025, first two lines of Feurle).

Regarding claims 10 and 21, Kurjanowicz teaches that said information is stored in a space accessible through one or more wordlines of said DRAM (col.8, lines 17-22 and lines 37-40).

Regarding claim 11, Kurjanowicz teaches that said information is generated by post-fabrication stress testing of said DRAM (it is taught as the information access mode signals is generated under the single cell per bit access mode and dual cell per bit access mode and also see page 6 of applicant's remarks filed on 11/25/2005).

5. Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurjanowicz., US 6,894,941 B2 B1 and Feurle et al., US 2003/0043674 A1, in view of Klein., US 6,838,331 B2.

Regarding claims 5 and 16, Kurjanowicz and Feurle teaches that said first portion is refreshed at said first rate and said second portion is refreshed at said second rate (see col.8, lines 22-27), Kurjanowicz and Feurle do not teach that both said first portion and said second portion operate in a mode selected from the group consisting of active mode and sleep mode. However, Klein teaches that both said first portion and said second portion (the memory cells in the DRAM) operate in a mode selected from the group consisting of active mode and sleep mode (col.2, lines 39-50).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Klein into Kurjanowicz and Feurle's memory system such as the memory cells in the DRAM operate in a mode selected from the group consisting of active mode and sleep mode because it will reduce the power consumed by a DRAM device during refresh in at least some operating modes without risking a loss of data stored in the DARM device (col.3, lines 36-54).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

6. Claims 7 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurjanowicz., US 6,894,941 B2 B1 and Feurle et al., US 2003/0043674 A1, in view of Caulkins., US 6,473,355 B2.

Regarding claims 7 and 18, Kurjanowicz and Feurle teach the claimed invention as shown above (claims 1 and 12), Kurjanowicz and Feurle do not teach that said information is stored in a non-volatile memory and accessed from said non-volatile memory for storage in said DRAM. However, Caulkins teaches said information is stored in a non-volatile memory and accessed from said non-volatile memory for storage in said DRAM (col.3, lines 40-44 and col.5, lines 9-12).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Caulkins into Kurjanowicz and Feurle's memory system such as said information is stored in a non-volatile memory and accessed from said non-volatile memory for storage in said DRAM because the non-volatile memory can maintain data for extended periods of time without any power being supplied to the device (col.1, lines 36-38) and the non-volatile memory also provides the stability and security (col.3, lines 23-24).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 19, Kurjanowicz teaches that said information is stored on one or more fuses on an integrated circuit including said DRAM (col.3, lines 34-36).

Response to Applicant's Arguments

7. Applicant's arguments filed on 05/24/2006 have been fully considered but they are not persuasive.

In response to applicant's arguments that neither reference nor the combination disclose accessing said stored information to determine when and to refresh said first portion at said first rate and to determine when and to refresh said second portion at said second rate in applicant's remarks, page 8, second paragraph, however, it is noted that Kurjanowicz teaches accessing said stored information to determine when and to refresh said first portion at said first rate (it is taught as cases 1 and 2 as shown in table 1; see col.9, lines 39-55; Kurjanowicz clearly teaches when to refresh the first portion at said first rate, for example, when SHORT-PG and DIFF_MODE are at the low logic level) and to determine when and to refresh said second portion at said second rate (it is taught as cases 8 and 9 as shown table 1, see col.10, lines 20-45; Kurjanowicz clearly teaches when to refresh the second portion at said second rate, for example, when SHORT-PG and DIFF_MODE are at the high logic level). Therefore, the references teaches the cited claim limitations as shown in claims 1 and 12

8. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 7:30-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jasmine Song

Patent Examiner

August 10, 2006